IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: John T. Moore

Patent No.: 6,967,383 B2

Issued: November 22, 2005

For: TRANSISTOR WITH NITROGEN-HARDENED GATE OXIDE

Attorney Docket No.: 2269-4308.4US

VIA ELECTRONIC FILING

October 5, 2007

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is noted that several errors appear in this patent of a typographical nature. These errors are due to mistakes in printing on the part of the U.S. Patent and Trademark Office, and occurred through no fault of the Applicants. A certificate of correction in the form attached hereto is requested.

Please note that an Amendment Pursuant to 37 C.F.R. § 1.312(a) (copy enclosed) was filed concurrently with the issue fee on April 27, 2005, but the amendments contained therein were apparently not completely entered before issuance of the patent. Attached is a copy of the previously filed Amendment Pursuant to 37 C.F.R. § 1.312(a) and the date-stamped postcard, acknowledging receipt by the PTO, to provide proof of such filing. We have included subject matter of this amendment on the attached PTO/SB/44 with at least one copy being suitable for printing.

Please send the Certificate to:

Name: James R. Duzan
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

Attached hereto is Form PTO/SB/44, which is suitable for printing.

Respectfully submitted,

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Date: October 5, 2007
JRD/df/lh

Attachments: PTO/SB/44
Copy of Amendment Pursuant to 37 C.F.R. § 1.312(a)
Copy of date-stamped postcard

Document in ProLaw

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO	:	6,967,383 B2
APPLICATION NO.:		10/791,400
ISSUE DATE	:	November 22, 2005
INVENTOR(S)	:	John T. Moore

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the specification:

COLUMN 5, LINE 28, after "FIG. 3," insert --is--

In the claims:

CLAIM 6, COLUMN 9, LINE 10, change "1," to --4,--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

James R. Duzan
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

John T. Moore

Serial No.: 10/791,400

Filed: March 2, 2004

For: TRANSISTOR WITH NITROGEN-HARDENED GATE OXIDE

Confirmation No.: 2554

Examiner: C. Wilson

Group Art Unit: 2829

Attorney Docket No.: 2269-4308.4US (99-1199.04/US)

Notice of Allowance Mailed:

January 27, 2005

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL994848733US

Date of Deposit with USPS: April 27, 2005

Person making Deposit: Steven P. Wong

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Specification appear on page 2 of this paper.

A **Listing of the Claims** begins on page 3 of this paper.

Remarks begin on page 7 of this paper.

IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a continuation of application Serial No. 10/010,025, filed December 6, 2001, ~~pending,~~ now U.S. Patent 6,747,327, issued June 8, 2004, which is a divisional of application Serial No. 09/585,688, filed June 1, 2000, now U.S. Patent No. 6,342,437, issued January 29, 2002.

Please amend paragraph number **[0024]** as follows:

[0024] After provision of the semiconductor substrate 10 having the gate oxide layer 12 formed thereover, the gate oxide layer 12 is subjected to a RPN treatment. The RPN treatment incorporates nitrogen into an upper area 14 (depicted in FIG. 2) of the gate oxide layer 12, resulting in a large concentration of nitrogen at the upper surface 13 of the gate oxide layer 12. ~~As is shown~~ Shown in drawing FIG. ~~3,~~ 3 is a graph of a binding energy analysis of the gate oxide layer 12 after the RPN ~~treatment, the~~ treatment. The nitrogen-containing upper area 14 of the gate oxide layer 12 includes unbound or interstitial nitrogen (indicated by the oxy-nitride peak 16) as well as silicon nitride (Si_3N_4) (indicated by the nitride peak 18).

IN THE CLAIMS:

None of the claims have been amended herein. All of the pending claims 1 through 14 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Original) A transistor, comprising:

a substrate;

a nitrogen-free polysilicon electrode contacting a portion of the substrate; and

a gate oxide disposed between the substrate and the nitrogen-free polysilicon electrode, the gate oxide including about 0.5% nitrogen by atomic weight at an interface with the substrate, the nitrogen progressively increasing to comprise between 2.5% and 10.0% nitrogen by atomic weight at an interface with the nitrogen-free polysilicon electrode, the gate oxide hardened using a remote plasma-based nitrogen hardening treatment and annealed thereafter.

2. (Previously presented) The transistor of claim 1, wherein the nitrogen-free polysilicon electrode has a bottom surface comprising a P-type dopant.

3. (Original) The transistor of claim 2, wherein the P-type dopant is boron.

4. (Original) A surface P-channel transistor, comprising:

a substrate;

a nitrogen-free polysilicon electrode contacting a portion of the substrate, the electrode comprising a P-type dopant including boron; and

a gate oxide disposed between the substrate and the nitrogen-free polysilicon electrode, the gate oxide including about 0.5% nitrogen by atomic weight at an interface with the substrate, the nitrogen progressively increasing to comprise between 2.5% and 10.0% nitrogen by atomic weight at an interface with the nitrogen-free polysilicon electrode, the gate oxide hardened using a remote plasma-based nitrogen hardening treatment and annealed thereafter.

5. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises a hardened gate oxide using the remote plasma-based nitrogen hardening treatment using a high density plasma process for approximately 60°C for about 10 seconds using about 1500 watts of power.

6. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises hardening the gate oxide using a thermal remote plasma-based nitrogen hardening treatment process at approximately 750°C for about 2 minutes.

7. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises a hardened gate oxide annealed at approximately 800°C for approximately 60 seconds.

8. (Previously presented) A transistor, comprising:

a substrate;

a nitrogen-free polysilicon electrode contacting a portion of the substrate; and

a gate oxide disposed between the substrate and the nitrogen-free polysilicon electrode, the gate oxide including essentially 0.5% nitrogen by atomic weight at an interface with the substrate, the nitrogen progressively increasing to comprise essentially in the range of between 2.5% and 10.0% nitrogen by atomic weight at an interface with the nitrogen-free polysilicon electrode, the gate oxide hardened using a remote plasma-based nitrogen hardening treatment and annealed thereafter.

9. (Previously presented) The transistor of claim 8, wherein the nitrogen-free polysilicon electrode has a bottom surface comprising a P-type dopant.

10. (Previously presented) The transistor of claim 8, wherein the P-type dopant includes boron.

11. (Previously presented) A surface P-channel transistor, comprising:

a substrate;

a nitrogen-free polysilicon electrode contacting a portion of the substrate, the electrode comprising a P-type dopant including boron; and

a gate oxide disposed between the substrate and the nitrogen-free polysilicon electrode, the gate oxide including essentially 0.5% nitrogen by atomic weight at an interface with the substrate, the nitrogen progressively increasing to comprise essentially in the range of between 2.5% and 10.0% nitrogen by atomic weight at an interface with the nitrogen-free polysilicon electrode, the gate oxide hardened using a remote plasma-based nitrogen hardening treatment and annealed thereafter.

12. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises a hardened gate oxide using the remote plasma-based nitrogen hardening treatment using a high density plasma process for essentially 60°C for about 10 seconds using essentially 1500 watts of power.

13. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises hardening the gate oxide using a thermal remote plasma-based nitrogen hardening treatment process at essentially 750°C for essentially 2 minutes.

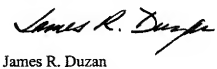
14. (Previously presented) The surface P-channel transistor of claim 4, wherein the gate oxide comprises a hardened gate oxide annealed at essentially 800°C for essentially 60 seconds.

REMARKS

This amendment corrects errors in the text. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,



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Date: April 27, 2005
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THE PATENT & TRADEMARK OFFICE MAILROOM DATE-STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Transmittal Letter (2 pages in duplicate); Part B-Issue Fee Transmittal (1 page); Check No. 21607 in the amount of $1715.00; Amendment under 37 C.F.R. § 1.312 (7 pages); Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages).

Invention:	TRANSISTOR WITH NITROGEN-HARDENED GATE OXIDE
Applicant(s):	John T. Moore
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